

FIG. 1

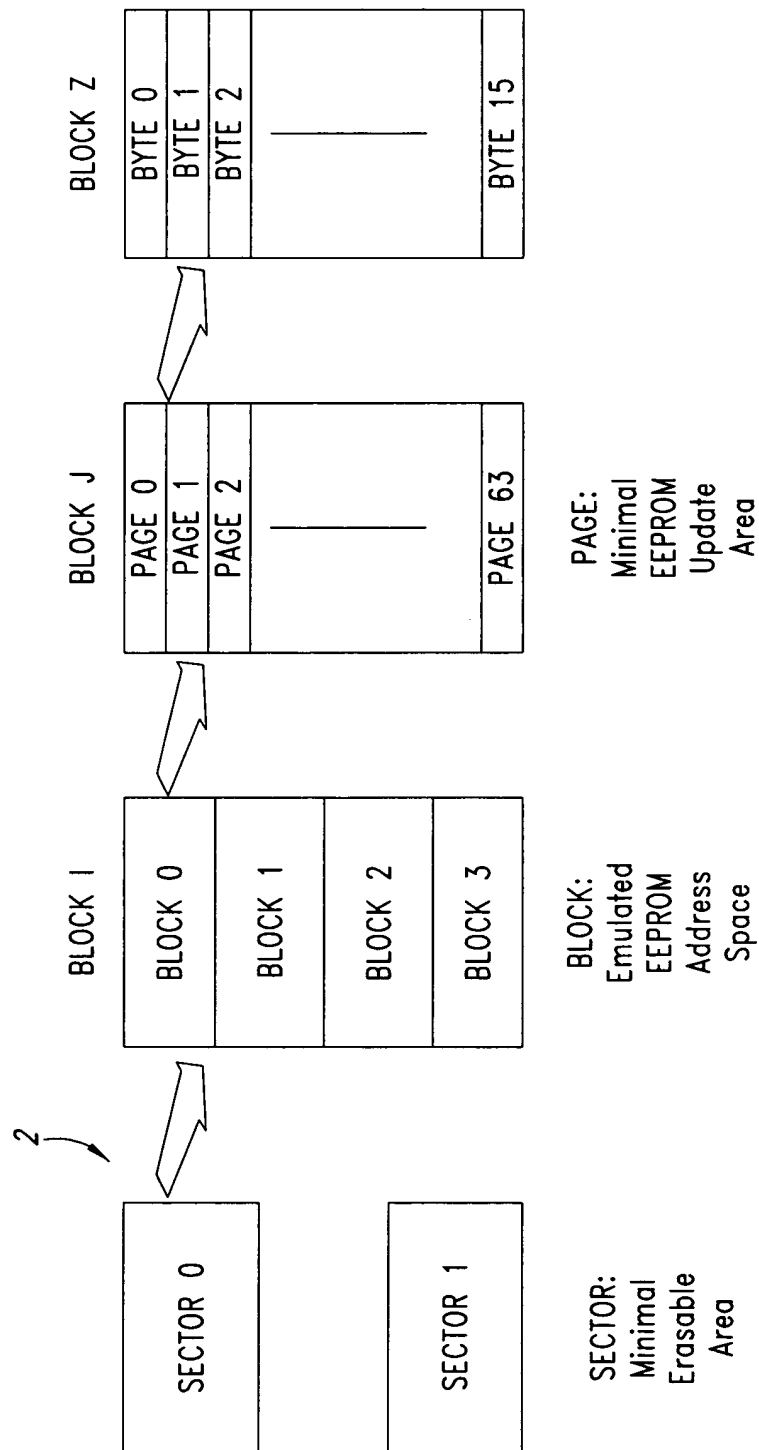


FIG. 2

Simplification: 4 pages (instead of 64) for each block

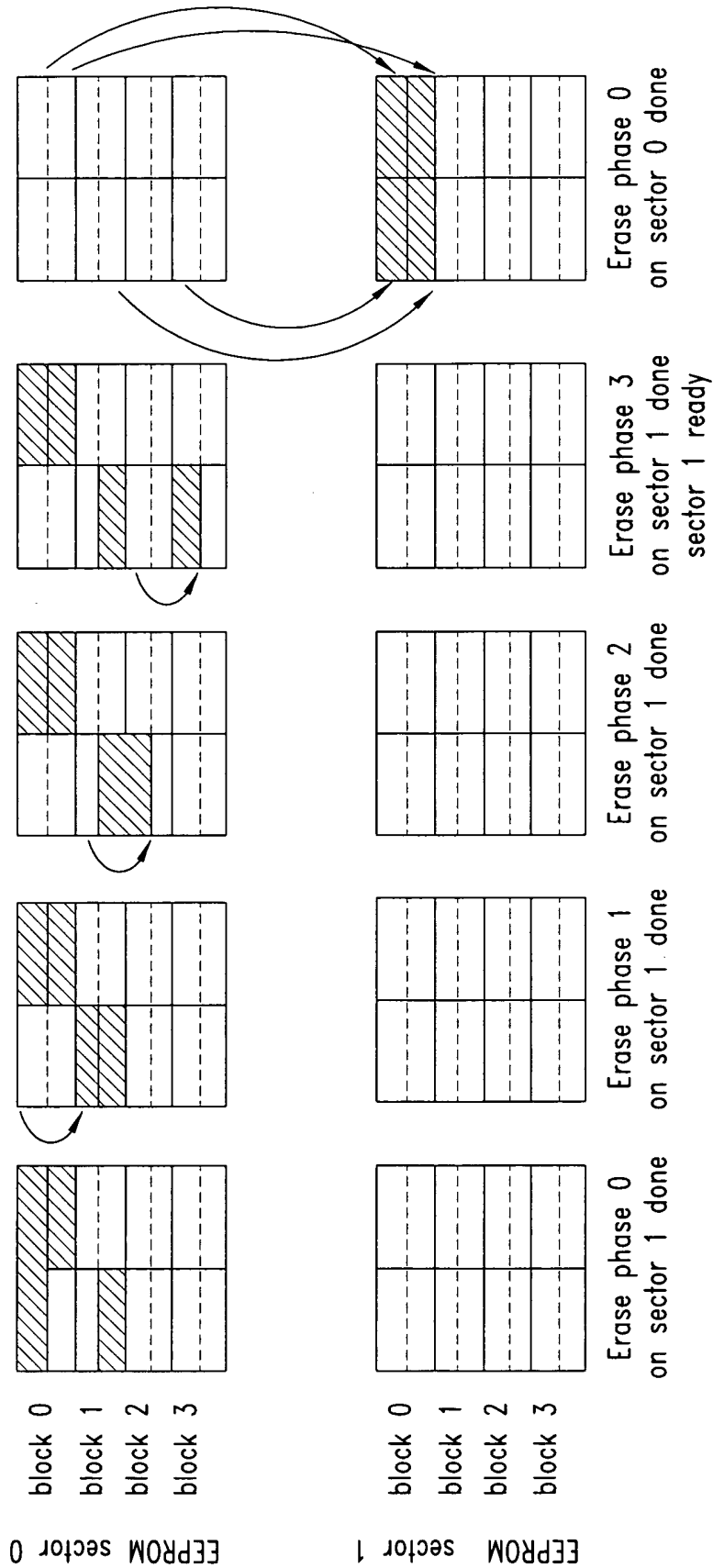


FIG. 3

224000h	FCR
224001h	ECR
224002h	FSR

FIG. 3A

Sector	Addresses	Max Size
OTP	211F80h to 211FFFh	128 byte
Flash 0	000000h to 00FFFFh	64 Kbyte
Flash 1	01000h to 01BFFFh	48 Kbyte
Flash 2	01C000h to 01DFFFh	8 Kbyte
Flash 3	01E000h to 01FFFFh	8 Kbyte
EEProm	220000h to 2203FFh	1 Kbyte

FIG. 3B

7	6	5	4	3	2	1	0
FWMS	FPAGE	FCHIP	FBYTE	FSECT	FSUSP	PROT	FBUSY

FIG. 3C

7	6	5	4	3	2	1	0
EWMS	EPAGE	ECHIP			WFIS	FEIEN	EBUSY

FIG. 3D

7	6	5	4	3	2	1	0
FERR	FSS6	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

FIG. 3E

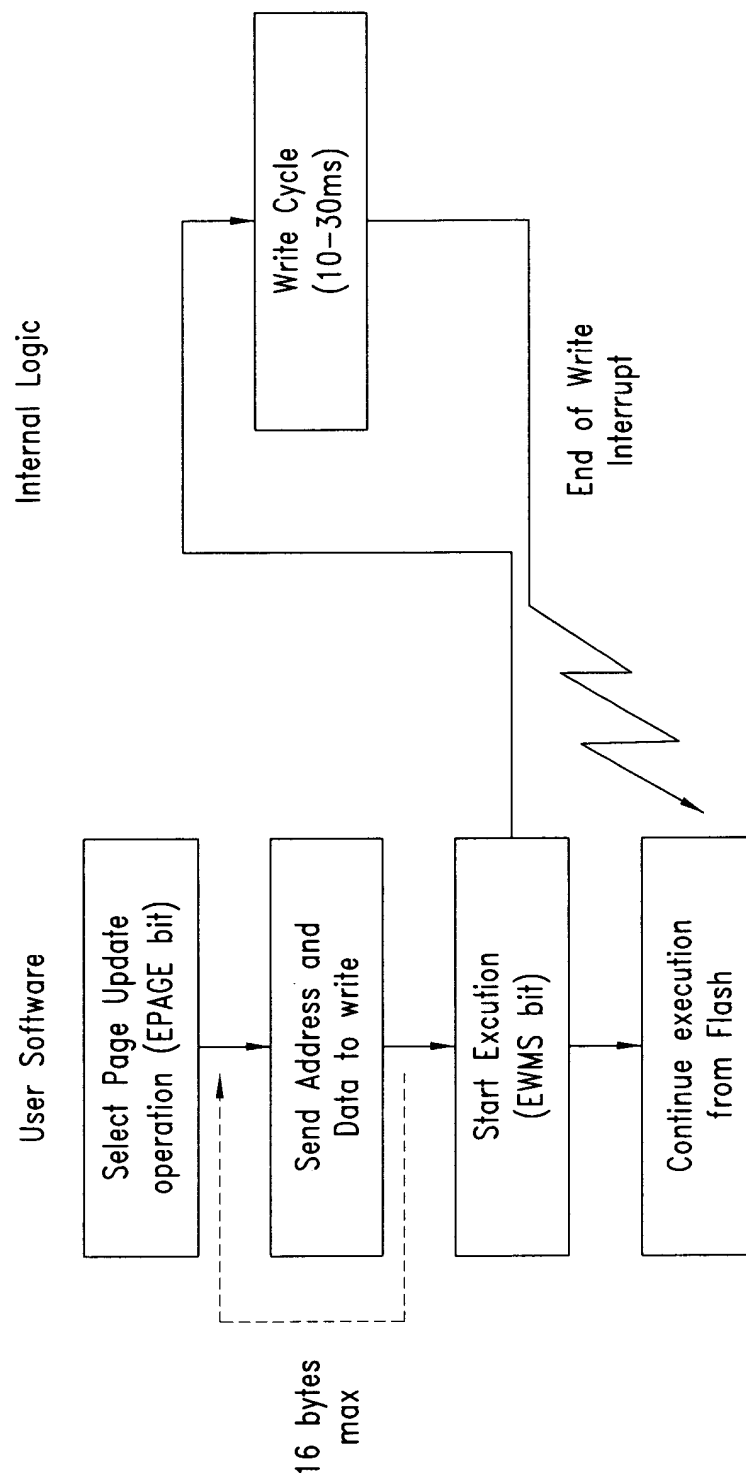


FIG. 4

211FFCh	NVAPR
211FFDh	NVWPR
211FFEh	NVPWD0
211FFFh	NVPWD1

FIG. 4A

Operation	Size	Min	Typ	Max
Page Update	256 byte	160 us	10 ms	30 ms
	512 byte	160 us	15 ms	50 ms
	1 Kbyte	160 us	30ms	100 ms
Chip Erase	256 byte		35 ms	100 ms
	512 byte		45 ms	150 ms
	1 Kbyte		70 ms	300 ms

FIG. 4B

7	6	5	4	3	2	1	0
APRA	APRO	APBR	APEE	APEX	PWT2	PWT1	PWTO

FIG. 4C

7	6	5	4	3	2	1	0
TMDIS	PWOK	WPBR	WPEE	WPRS3	WPRS2	WPRS1	WPRS0

FIG. 4D

7	6	5	4	3	2	1	0
PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0

FIG. 4E

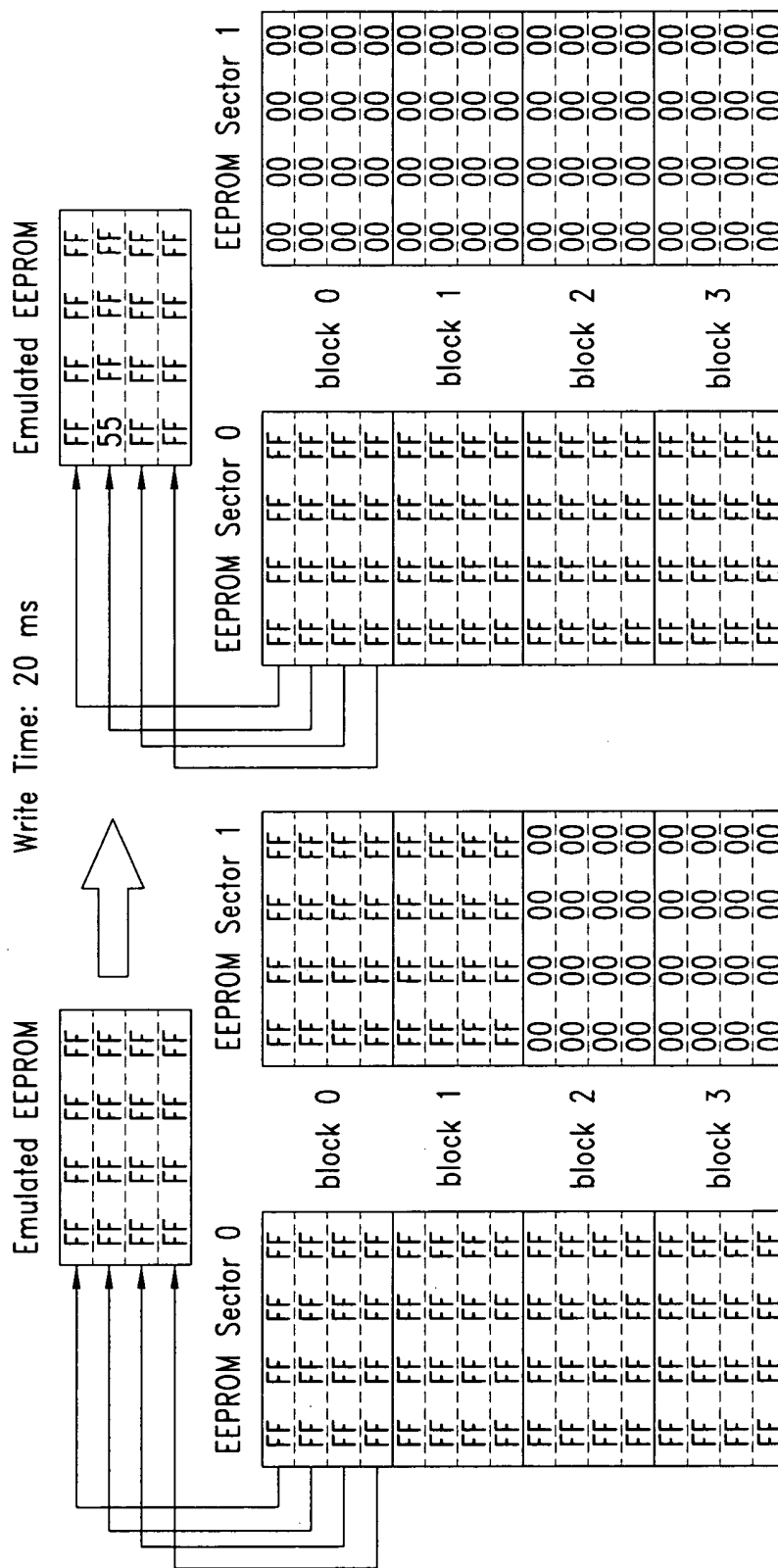


FIG. 5

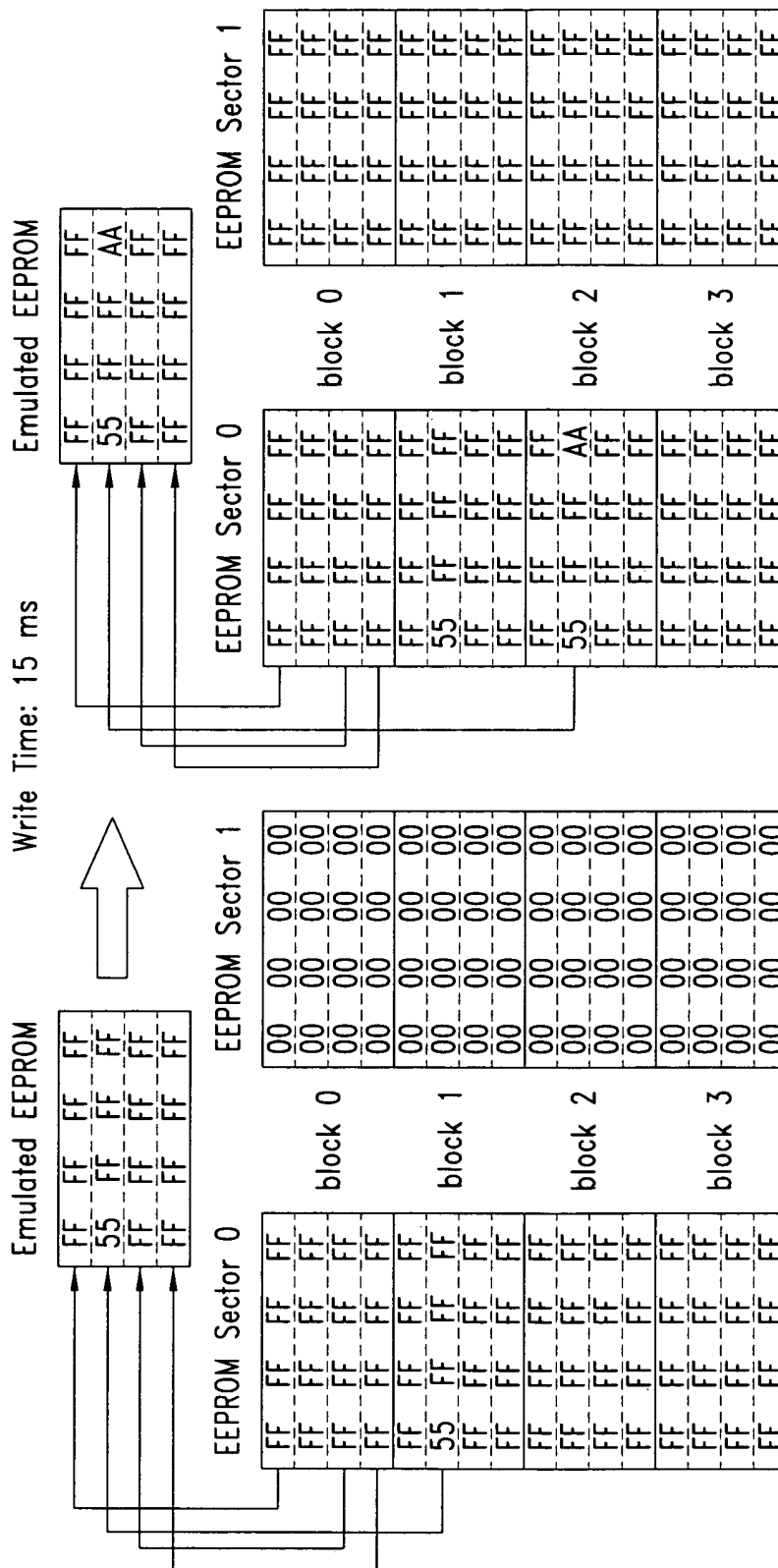


FIG. 6

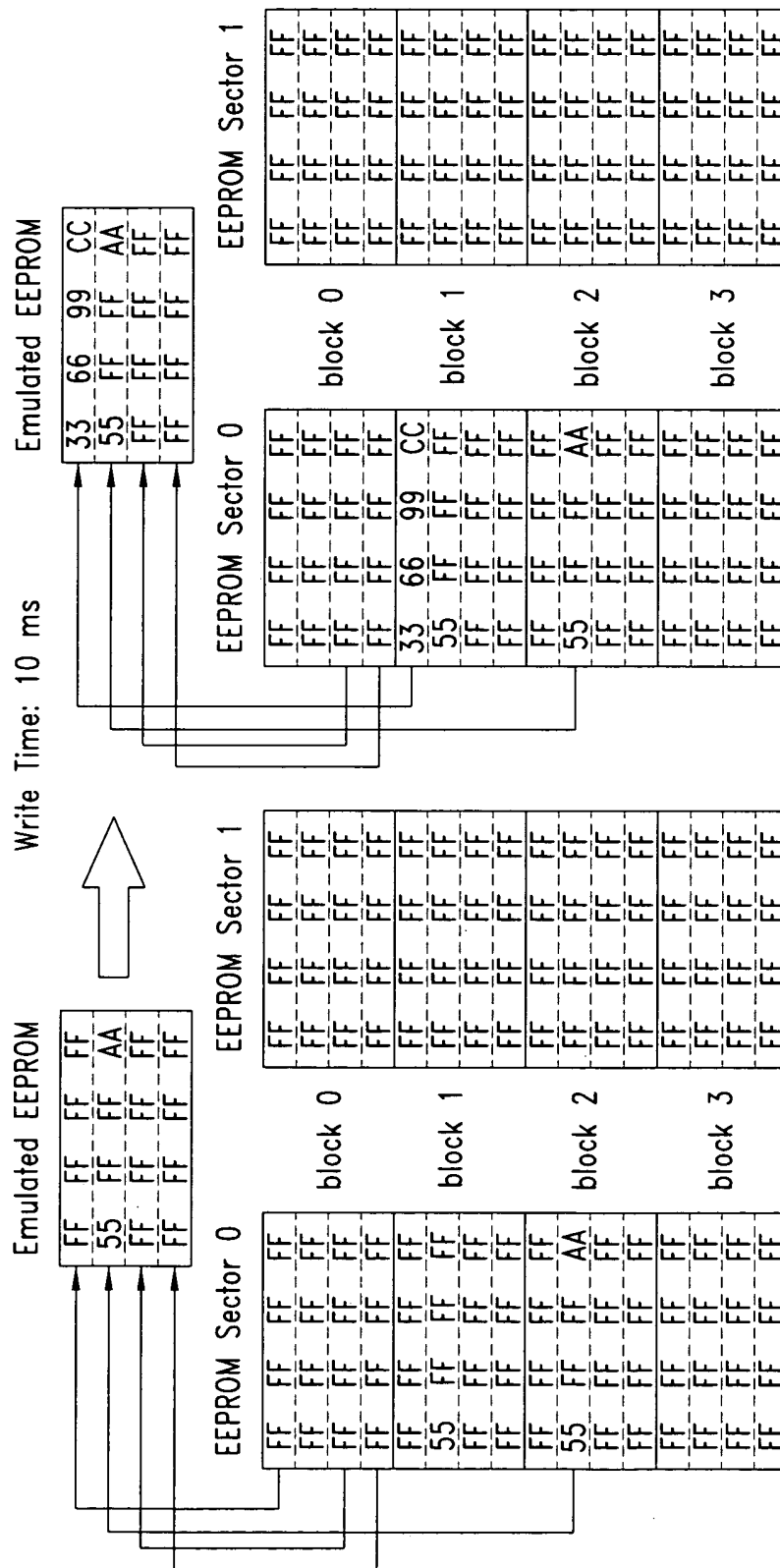


FIG. 7

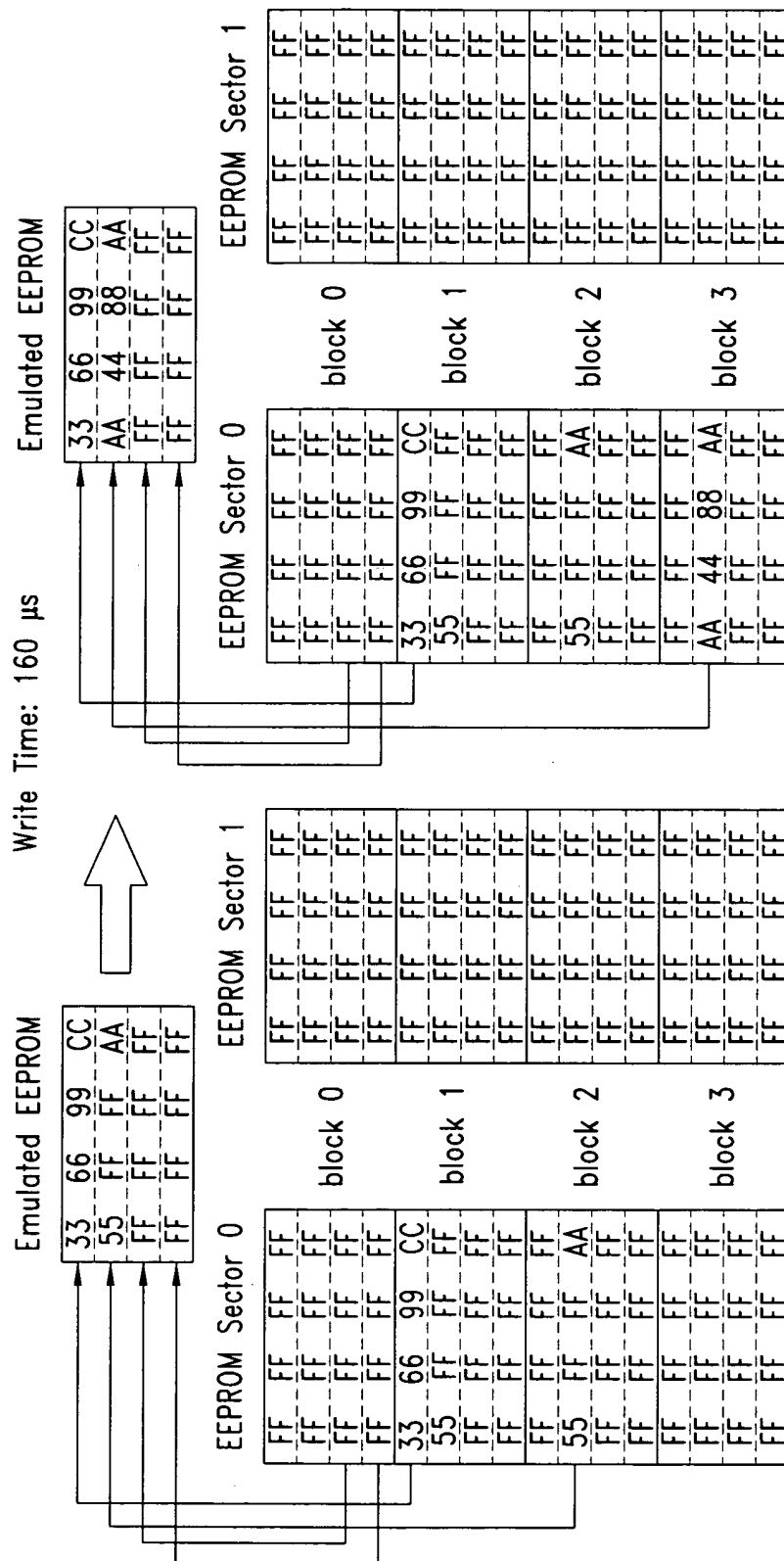


FIG. 8

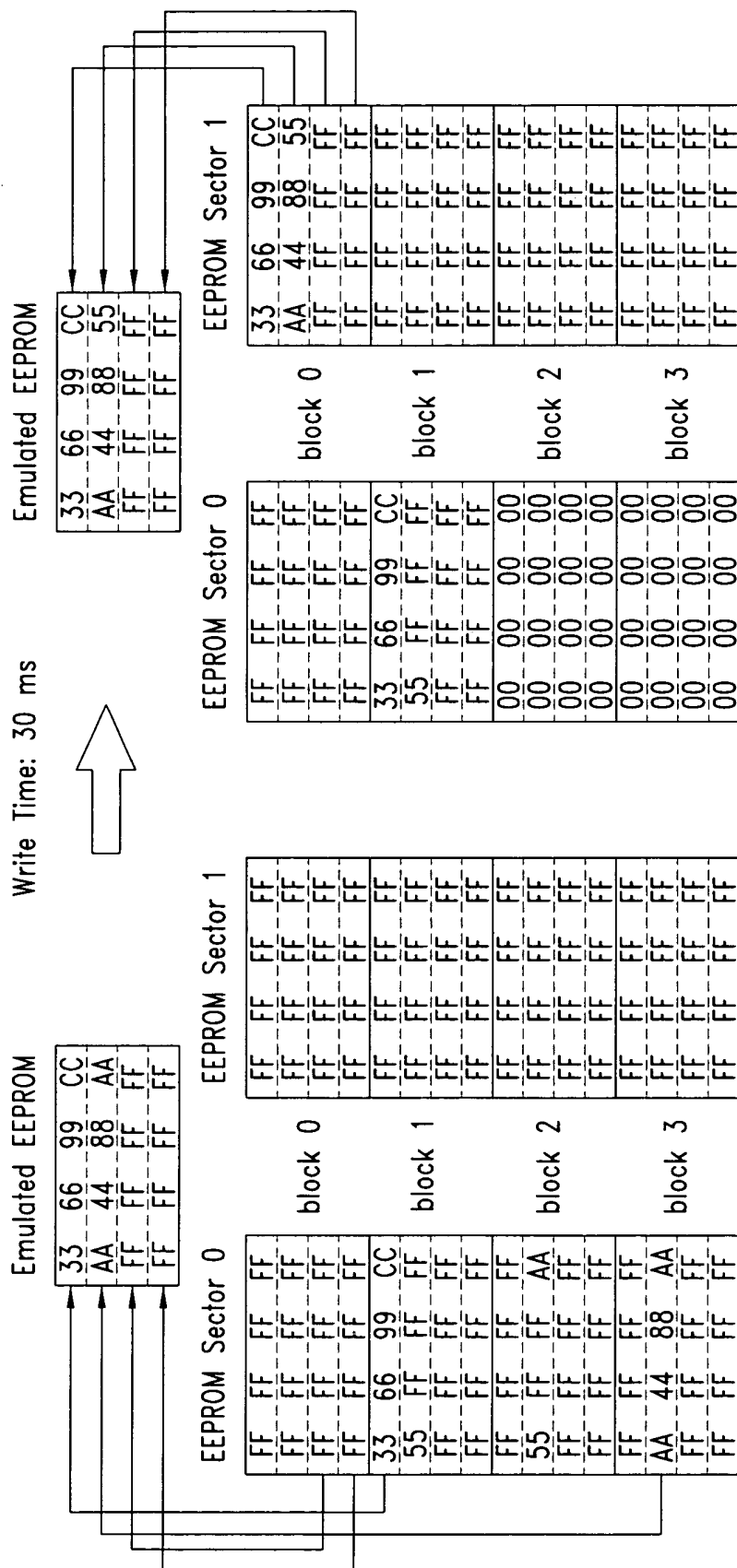


FIG. 9

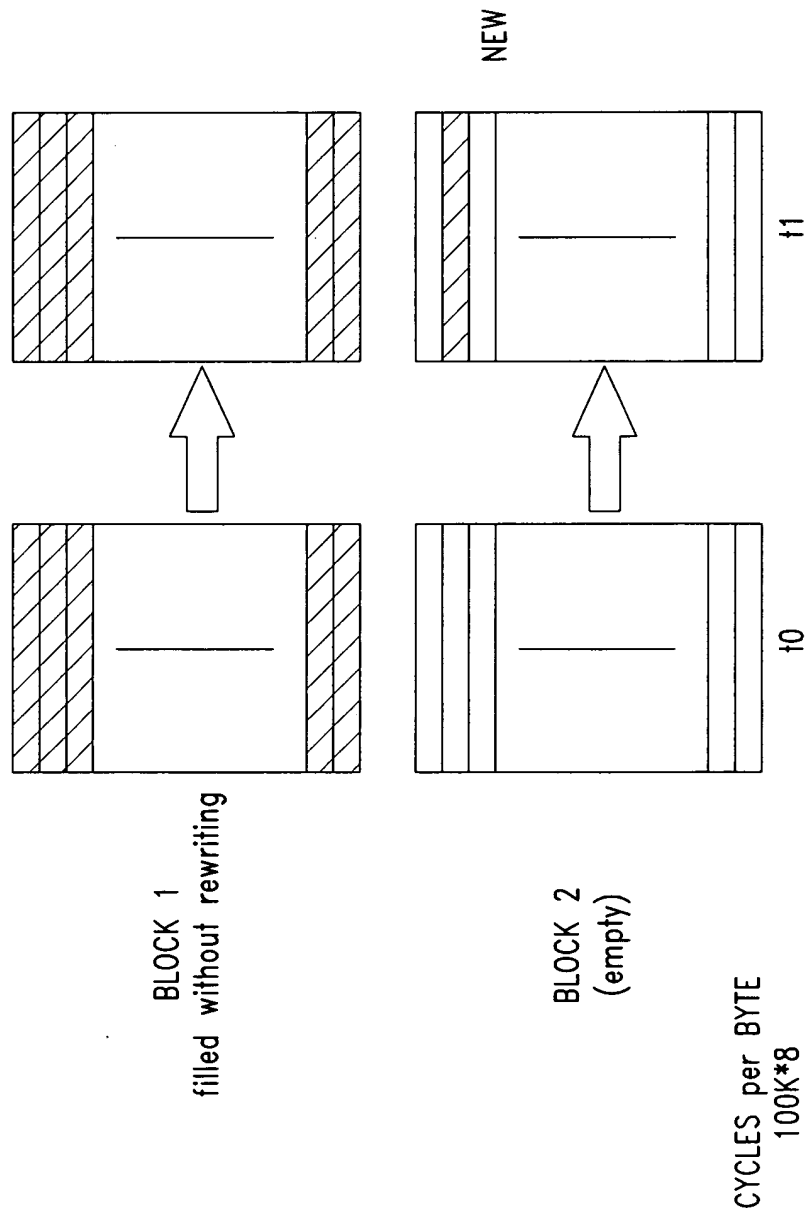


FIG. 10

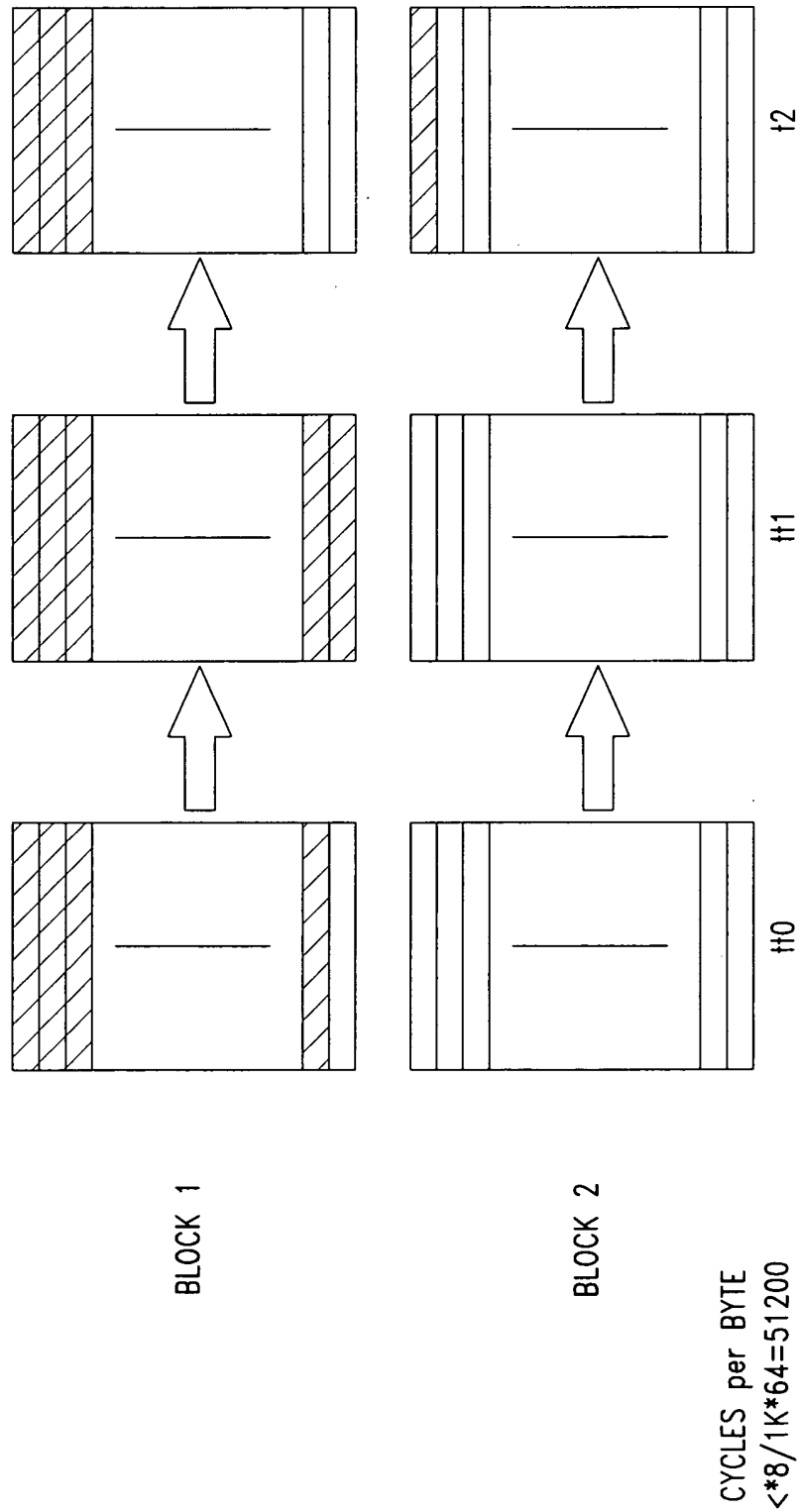


FIG. 11

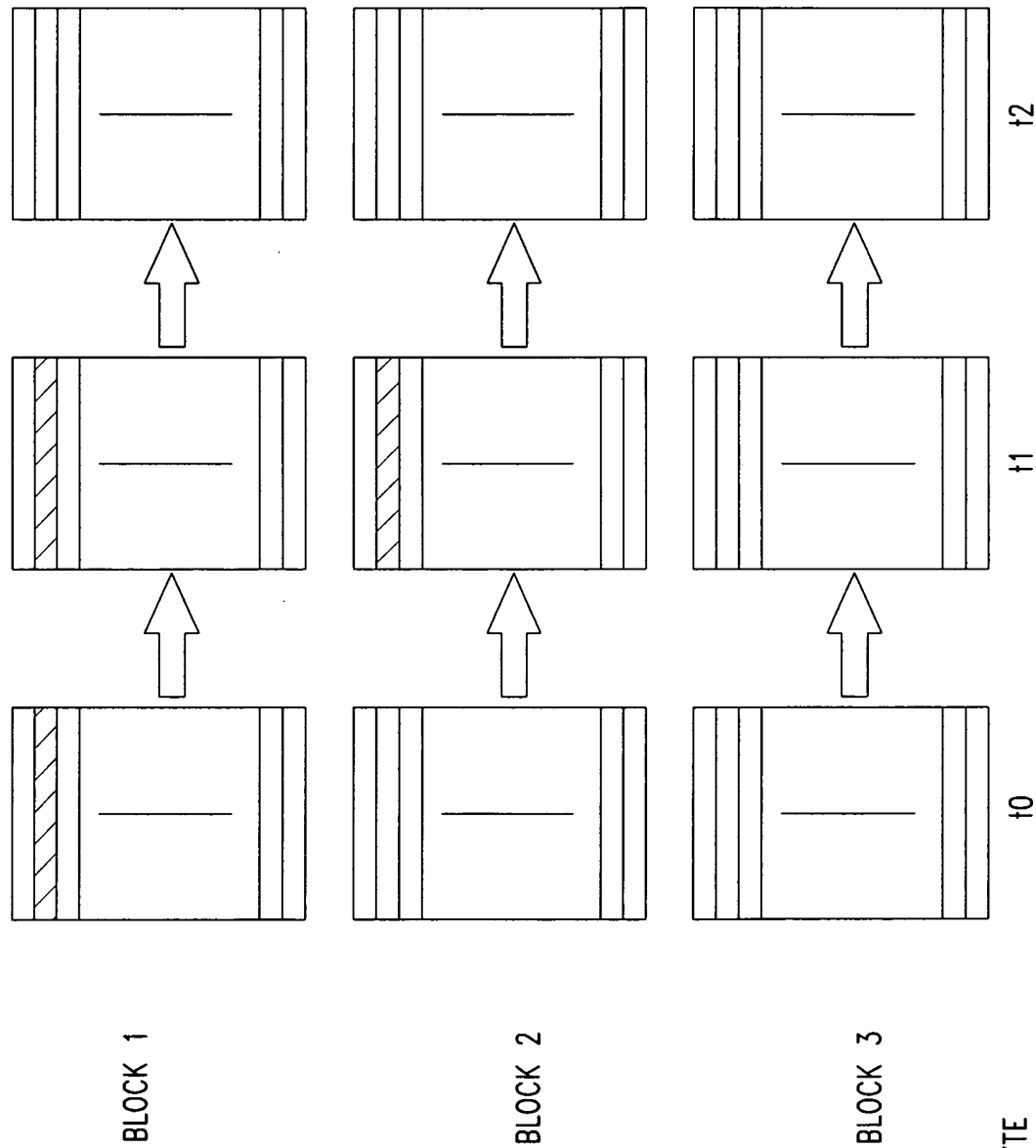


FIG. 12

CYCLES per BYTE
 100K*8/1K=800

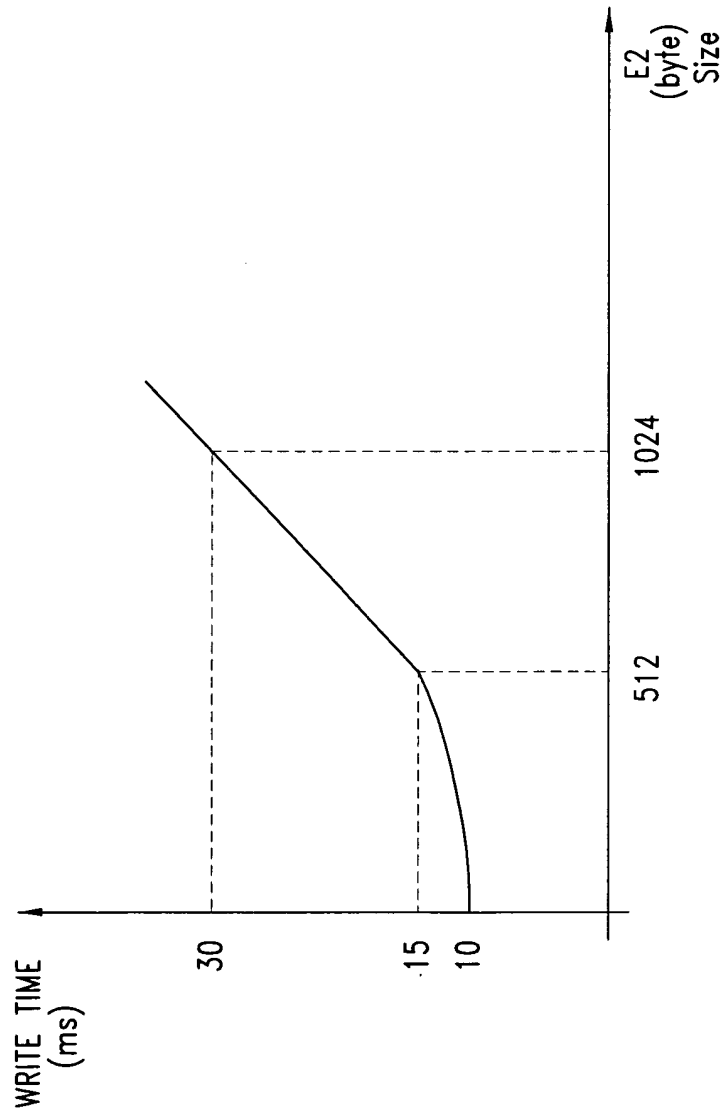


FIG. 13

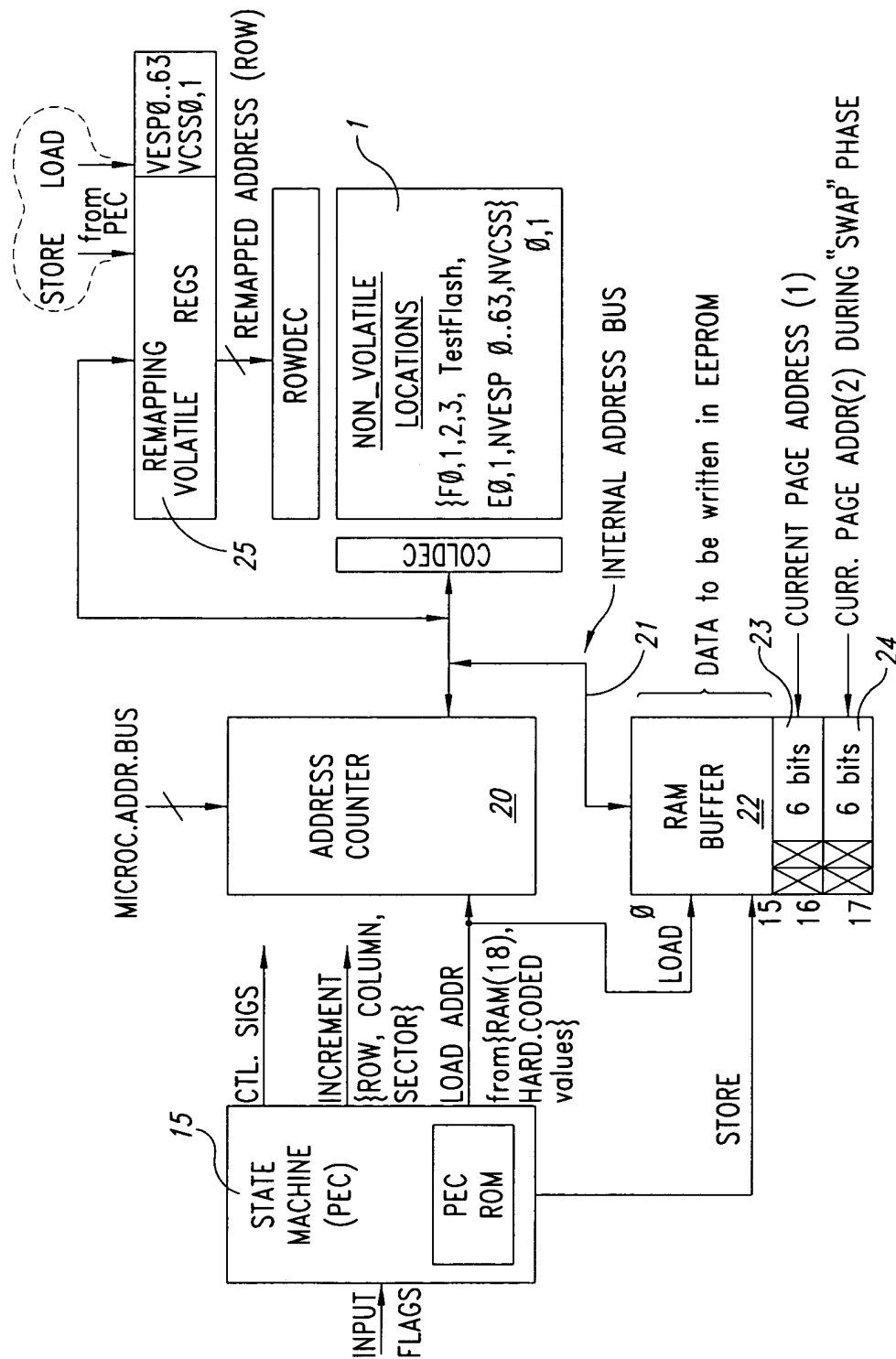


FIG. 14